ECR #: 34
Title: Address re-mapping on PCI port
Release Date: May 12, 1997
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary: Need to clarify how PCI accesses through a non A.G.P. (PCI) port are handled

Background: This ECR provides a clarifying replacement for the "Address re-mapping" paragraph in section 2.4..

Change Current Specification as shown:

Replace the subject paragraph with the text below, including associated footnotes.

Address re-mapping support for PCI compliant bus master accesses to memory: GART range address re-mapping support is provided by the chipset for graphics devices attached to the A.G.P. interface. Re-mapping support is, in general, **not** provided for devices attached to standard PCI bus(es). However, to provide a consistent addressing model across the system, this interface specification ***requires*** the following processor dependent[1], address re-mapping support for accesses presented at a PCI port. 1) Chipsets that allow the processor to generate physical addresses in the GART range (i.e., GART address re-mapping is supported for processor accesses as well as for A.G.P. accesses) ***must*** support an identical re-mapping service for the PCI port. 2) Chipsets that do not support re-mapping for processor accesses (i.e., the processor resolves its own GART range addresses to valid physical memory ranges) must NOT do any re-mapping of addresses presented at the PCI port.

In the case where GART re-mapping is not provided at the PCI port, any address in the GART address range that is presented at the PCI port must be deemed an access error, and dealt with consistent with the error handling policies of that platform. In general, out of bounds or otherwise erroneous PCI requests do not receive any response and result in a master abort. In ***NO*** case may an address falling in the GART range be propagated through the core logic without re-mapping.

Device drivers managing PCI bus master devices should always use the standard system call to de-reference addresses being passed to the hardware. This will guarantee that the correct address is used for the current platform and level of chipset support. Conversely, device drivers managing A.G.P.-enabled bus master devices should always de-reference virtual addresses via the new or alternate system call associated with the new A.G.P. VMM services described in the Memphis DDK. This will guarantee that the linear GART address is always used on the A.G.P. port, independent of platform differences described here. PCI bus master device drivers should never use this new de-referencing call.

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[1] The chipset implementation of GART re-mapping is related to the memory management implementation of the attached processor, including, for example, the behavior of MTRRs. However, this reference to processor implementation is made as an example for clarification purposes only. This specification does not place any requirements on processor behavior, nor stipulate any particular processor behavior.